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PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM 10082055	FILING DATE 02/26/2002	CLASS 302 343-	SUBCLASS 117	GAU 2473	EXAMINER Raymond
**APPLICANTS: Gotoh Kohtaroh; Aoyagi Koji; Terashima Kazuhiro; Nishio Shigeru; 2857					
**CONTINUING DATA VERIFIED:					
** FOREIGN APPLICATIONS VERIFIED: JAPAN 2001-269216 09/05/2001					
PG-PUB DO NOT PUBLISH <input type="checkbox"/>		RESCIND <input type="checkbox"/>			
Foreign priority claimed <input type="checkbox"/> yes <input type="checkbox"/> no		35 USC 119 conditions met <input type="checkbox"/> yes <input type="checkbox"/> no		ATTORNEY DOCKET NO 100021-00072	
Verified and Acknowledged Examiners's initials					
TITLE : Test circuit and semiconductor integrated circuit effectively carrying out verification of connection of nodes					
U.S. DEPT. OF COMM /PAT. & TM-PTO-435L (Rev. 12-94)					

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NOTICE OF ALLOWANCE MAILED		Assistant Examiner		CLAIMS ALLOWED	
				Total Claims	Print Claim for O.G.
ISSUE FEE		Primary Examiner		DRAWING	
Amount Due	Date Paid			Sheets Drwg.	Figs. Drwg.
<input type="checkbox"/> TERMINAL DISCLAIMER		PREPARED FOR ISSUE		Application Examiner	
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